

 **B.Tech VLSI-2017 MINI Projects**

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| Front End Design(VHDL/Verilog HDL) |
| S.No | Project Name |
| 1 | Implementation of Dadda Algorithm and its applications  |
| 2 | Area efficient Image Compression Technique using DWT |
| 3 | High speed and Area efficient Radix-8 Multiplier for DSP applications |
| 4 | Error Protection Scheme For Registers(*Self Immunity Technique*) |
| 5 | Design and implementation of LUT using APC-OMS Technique  |
| 6 | Parallel prefix adders for cryptographic applications |
| 7 | Design and Implementation of DES |
| 8 | Synthesis Techniques for Pseudo-Random Built-In Self-Test Based on the LFSR |
| 9 | Power Optimization of Linear Feedback Shift Register LFSR) for Low Power BIST implemented in HDL |
| 10 | Area efficient concurrent error detection and correction for parallel filters |
| 11 | Design of Optimized Reversible Multiplier for High Speed DSP Application |
| 12 | Interfacing Synchronous and Asynchronous Domains for Open Core Protocol |
| 13 | Implementation of CRC on FPGA |
| 14 | Low power and area efficient Wallace tree multiplier using carry select adder with binary to excess-1 converter |
| 15 | Design of Anti-collision Technique for RFID UHF Tag using Verilog |
| 16 | Low Power Compressor Based MAC Architecture for DSP Applications |
| 17 | A Very Fast and Low Power Carry Select Adder Circuit |
| 18 | Multiplication Acceleration Through Twin Precision |
| 19 | Designing Efficient Online Testable Reversible Adders With New Reversible Gate |
| 20 | Performance of Low Power BIST Architecture for UART |
| 21 | Single phase clock distribution using VLSI technology for low power |
| 22 | High Speed FPGA implementation of FIR Filters for DSP Applications |
| 23 | Implementation of an Efficient Multiplier based on *Urdhva Tiryakbhyam Sutra*  |
| 24 | LUT Optimization for Memory-Based Computation  |
| 25 | Design and implementation of Floating Point Multiplier based on Vedic Multiplication Technique |
| 26 | Efficient VLSI Implementation of DES and Triple DES Algorithm with Cipher Block Chaining concept using Verilog and FPGA |
| 27 | Constant and high speed adder design using QSD number system |
| 28 | FPGA implementation of multi operand redundant adders |
| 29 | A Novel Approach for parallel CRC generation for High Speed Application |
| 30 | A Common Boolean Logic(CBL) implementation for modified CSLA |
| 31 | Implementation of Bus Bridge between AHB and OCP |
| 32 | An Efficient Implementation of Floating Point Multiplier |
| 33 | A New Approach To Design Fault Coverage Circuit With Efficient Hardware Utilization for Testing Applications |
| 34 | Area Efficient parallel FIR Digital Filter Structures for Symmetric Convolution based on Fast FIR Algorithm |
| Back End Design |
| 35 | Recursive Approach To The Design of A Parallel Self-Timed Adder |
| 36 | Low power area efficient ALU with low power full adder |
| 37 | Comparative analysis and optimization of active power and delay of 1-bit full adder at 45nm technology |
| 38 | Statistical Analysis of MUX-Based Physical Unclonable Functions |
| 39 | Low power 6T SRAM design |
| 40 | Realization of Basic Gates Using MUX in CMOS Designs |
| 41 | Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator |
| 42 | CMOS Full-Adders for Energy-Efficient Arithmetic Applications |
| 43 | Low power design of Flip flop using reversible logic |
| 44 | Area Efficient ROM-Embedded SRAM Cache |
| 45 | Low power design of ripple carry adder |

**KREST TECHNOLOGIES**,

**Telangana**:Head Office, 2nd Floor, Solitaire Plaza, Beside Image Hospital, Ameerpet, Hyderabad.

 PH NO: 040-4443 3434,

Dilsukhnagar Ph: 9000404181,

Warangal Ph: 9000739460

 **Andhra Pradesh:** Vijayawada: Ph: 9000404182,

 **Tirupati:** Ph: 0877-6061111, 7207208081,

 **Maharastra** : Pune: Ph: 9763602006

 Nagpur: Ph: 9145532006